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WHITE PAPER

CIRCUIT LEVEL AGING SIMULATIONS PREDICT THE LONG-TERM BEHAVIOR OF ICS

HOW TO MINIMIZE DESIGN MARGINS WITH ACCURATE ADVANCED TRANSISTOR DEGRADATION MODELS

Reliability is a major criterion for integrated circuits (ICs) in safety critical applications, such as automotive, medical, or aviation electronics. A particular effect that contributes to wear-out is device (i.e. transistor) degradation. Its impact on the circuit behavior can be verified by circuit level aging simulations, which are offered by various EDA vendors. However, reasonable results can only be achieved with accurate and efficient device (i.e. transistor) degradation models. This white paper discusses the state of the art and points out opportunities for improvements.

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PRINCIPLES OF AGING SIMULATION

While IC design has always been addressing multiple design objectives, reliability has recently emerged as a major criterion. Safety critical applications that require long product lifetimes at, partially, 24/7 operation, for example in automotive, medical, aviation, or industrial applications, are the main commercial drivers of this trend.

Today, many safety critical applications demand compute capabilities that can only be provided by advanced technology nodes. Furthermore, extended technology options allow integrated high voltage (HV) devices to offer completely new system solutions.

However, advanced technology nodes and integrated HV devices are especially susceptible to device degradation, which cause gradual shifts in the transistor characteristics due to their degradation. The most well-known physical effects are hot carrier injection (HCI) as well as negative and positive bias temperature instability (NBTI / PBTI). HCI occurs in NFETs and PFETs due to drain currents. NBTI and PBTI are triggered by high gate voltages at elevated temperatures. While NBTI occurs in PFETs, PBTI occurs in NFETs and is only significant in high-k metal gate technologies. In reality, combinations of HCI and BTI may become relevant as well.

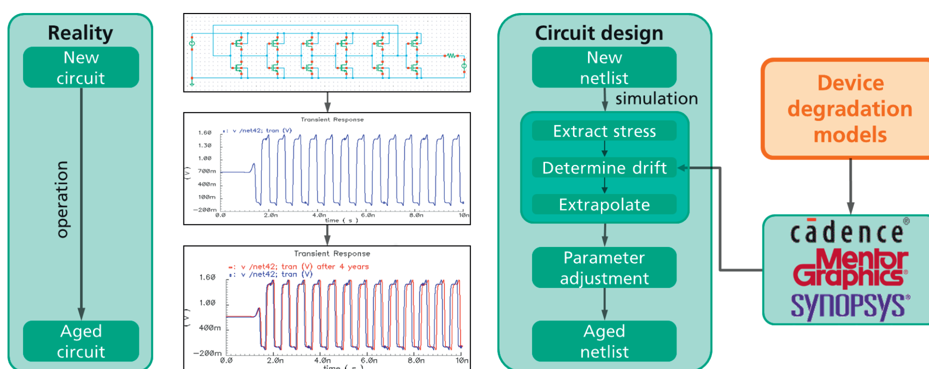

Figure 1: General flow of circuit level aging simulations

To support designers in verifying their reliability targets, EDA vendors offer circuit level aging simulation features, which follow the flow in Figure 1. The fresh circuit is simulated under a typical use scenario. From this simulation, voltages and currents are extracted for each transistor under investigation, and device degradation models compute the drifts of predefined device parameters due to aging. A netlist of the aged circuit is generated by adjusting these parameters in the simulation setup, and its simulation yields the behavior of the aged circuit.

It is obvious that device degradation models are major input variables and significantly impact the simulation outcome. With their tools, EDA vendors deliver, more or less simplistic, and potentially confidential built-in device degradation models that are not compatible between different vendor's environments. However, custom models can be implemented into the available vendor's reliability interfaces: Cadence URI, Synopsys MOSRA, Mentor Graphics

UDRM, and the emerging TMI/OMI. This white paper discusses the extension of design environments with advanced transistor degradation models, enabling the accurate prediction of device aging, and the reduction of design margins independent of the vendor's environment.

WAFER LEVEL RELIABILITY INVESTIGATION

Reliability has been a quality criterion for semiconductor technologies for a long time already. It has been monitored by wafer level reliability (WLR) measurements, for instance for process qualification [1]. Relatively large stress in terms of constant voltages (DC stress) and temperatures is applied to dedicated test structures, for instance single transistors in the scribe line to accelerate the degradation. During long-term measurements (up to days or weeks), the degradation of transistor performance characteristics, such as threshold voltage or saturation current, over time is recorded. Empirical models, such as [2]

$$\Delta p = k \cdot t^n,$$

describe HCI, NBTI, or PBTI measurement results by expressing the shift of a device characteristic p in a power-law dependence of the stress time t with an empirical exponent n. The factor k in this equation is a function of, e.g., gate-source voltage V_{gs}, drain-source voltage V_{ds}, temperature T, or device geometry. Its dependences are usually modeled by a product ansatz, such as in the NBTI model [2]

$$\Delta p = A_0 \cdot exp\left(\frac{E_{aa}}{k_B \cdot T}\right) \cdot \left(|V_{gs}|\right)^m \cdot t^n.$$

Especially in advanced technologies, where saturation has to be taken into account and input variables cannot be treated separately, more complex lifetime estimations are necessary. For example, [3] reported voltage-dependent time exponents n for NBTI and PBTI. Furthermore, the recovery of BTI degradation after reducing the stress in non-constant stress scenarios requires more complex models as well.

In general, WLR models allow measurements of overstressed operating conditions to be extrapolated on to normal operating conditions in an application thus predicting the lifetime of a single transistor based on fixed end-of-life criteria, for instance a 10 % shift in current or a certain absolute shift in threshold voltage. However, fixed end-of-life criteria for single devices do not represent the degradation of a whole circuit. Instead, it is necessary to consider the joint degradation of all transistors in a circuit to achieve an accurate lifetime prediction of the circuit.

PROPERTIES OF DEVICE DEGRADATION MODELS FOR AGING SIMULATIONS

While WLR measurements and models are tailored to single devices, circuit level

aging simulations investigate the behavior of an IC (or parts) with respect to the performance specifications under typical use scenarios. From this property, multiple requirements for device degradation models can be derived. First, each device in the circuit contributes differently to circuit degradation and experiences an individual transient stress in terms of voltages and currents. Both aspects, individual and transient stress per device, have to be taken into account. Second, circuit lifetimes in the range of years and simulation times in the range of $\ll 1\,s$ differ by multiple orders of magnitude. Aging simulations account for this by assuming use scenarios, so-called mission profiles, to be periodically repeated over the circuit lifetime. Stress and device degradation are determined during one period and extrapolated to the target age. This extrapolation has to be kept in mind during the definition of the degradation models. Third, device degradation models have to be implemented for the targeted simulation tool in-order to enable reasonable analysis runtimes.

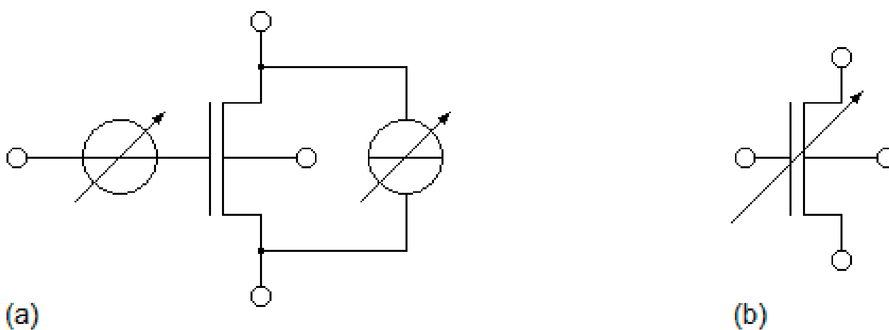

Figure 2: Implementation of device degradation models;
(a) (example for) subcircuit implementation; (b) model card approach

Independent of their detailed definitions, device degradation models for circuit level simulations can be implemented in two ways. Subcircuit models, such as the example in Figure 2(a), consider the transistor itself to be time-invariant but mimic its degradation by controlled sources. This approach is independent of the underlying device model, but it might be difficult to include all physical dependencies. As an alternative, the compact model parameters of the transistor can be adapted to express device degradation, which is indicated in Figure 2(b). This approach can benefit from directly using the built-in physics background of the compact model. However, the selection of compact model parameters to express device degradation depends on the underlying compact model and, potentially, on the technology.

DEVICE DEGRADATION MODELING AT FRAUNHOFER IIS/EAS

The modeling team at Fraunhofer IIS/EAS addresses device degradation and offers solutions to the open issues that have been hindering the wide-spread use of aging simulations in IC design and verification.

Support of Multiple Design Environments and EDA Tools
Independent of their detailed definition, device degradation models can be implemented into Cadence URI, Synopsys MOSRA, and Mentor Graphics UDRM

interfaces. In addition to this, Fraunhofer works towards supporting the emerging TMI/OMI interface.

This concept makes aging simulations in different environments compatible. Foundries will not need to separately support multiple design environments, and designers will be able to stick to their environments, usually without large adaptations.

Empirical Device Degradation Models based on DC WLR data

Two important properties of empirical WLR models were outlined above: DC stress conditions and overstress. Nevertheless, these models can be transferred into device degradation models for simulations under certain assumptions: extrapolation to normal use conditions and transfer to transient stress conditions by applying linear damage accumulation. This approach can be performed for HCI, NBTI and PBTI, or combinations of them.

Depending on the technology, the available data, and customer requirements, transistor degradation models can be implemented using a subcircuit or model card approach. Thereby, the resulting device degradation models for circuit level aging simulations are equally available in multiple design environments.

Physics-based Advanced NBTI Compact Model

Defects in the gate dielectric and at its interface to the transistor channel are considered the root cause of NBTI in PFETs [4]. During operation, the defects can be charged (charge trapping) or discharged (charge de-trapping). While charge trapping leads to degradation, mainly to an increase in the absolute threshold voltage of a transistor, charge de-trapping leads to recovery. The number of defects, their energetic properties, and the probabilities of charge trapping and de-trapping under various stress conditions are specific for a particular manufacturing process.

In Fraunhofer's physics-based NBTI compact model for circuit level aging simulations, the above effects are considered and abstracted to achieve high accuracy and numerical efficiency. The compact model naturally applies to transient, i.e. time-dependent or analog, stress and accounts for degradation including saturation and recovery [6].

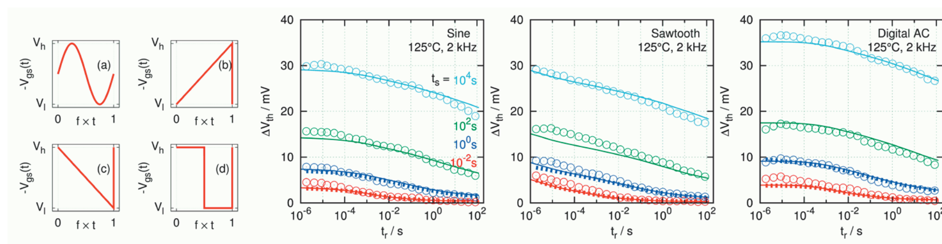

Figure 3: Experimental verification of the NBTI compact model. Measure-stress-measure experiments apply analog stress voltages (sine, sawtooth, inverse sawtooth, digital AC, (a) to (d) resp.) during a particular stress time and then measure the relaxation transients of the threshold voltage (right three plots). The compact model predictions (solid lines) are in good agreement with the experimental results (symbols) and the TCAD predictions (thick dashes, available only for smaller stress times). Different colors correspond to different stressing times ranging from $10^{-2}s$ *to* $10^{4}s$.

For verification, different analog stress scenarios in terms of signal shapes and stress durations are applied to single PFET devices. Figure 3 compares the corresponding recovery traces that can be observed in silicon measurements, TCAD simulations, and evaluations of the NBTI compact model. Their good agreement (deviations within 5 %) demonstrates the accuracy of the compact modeling approach [6].

As a demonstration example, the NBTI compact model was used in circuit level aging simulations of an operational amplifier. Transient asymmetric stress was applied to the input stage in Figure 4 (left) and leads to asymmetric degradations of the input transistors. As a result, a drift in the offset voltage of the operational amplifier can be observed. More simplistic models significantly over-estimate the degradation and lead to large margins that are required to meet the design objectives [6].

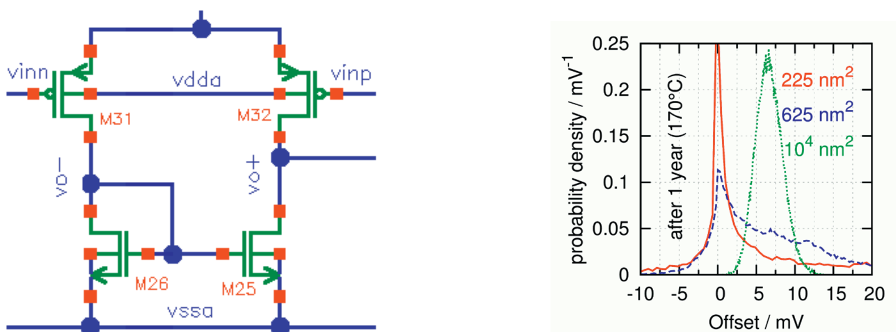

Figure 4: Application of the NBTI compact model to the input stage of an operational amplifier (left). The NBTI compact model provides access to NBTI variability, for instance to determine the probability density function of the offset voltage of the operational amplifier after 1 year of operation at elevated temperature). Different lines correspond to different PFET sizes (WxL) in the differential input stage: larger FETs lead to a Gaussian-like distribution function. Small FETs lead to a distribution function with a peak at zero offset and large tails.

Since charge trapping and de-trapping are stochastic processes, NBTI degradation is statistical in nature [7]. This NBTI compact model can account for the number of defects per transistor and the fact that their individual properties are random quantities. Therefore, it allows access to the circuit level impact of NBTI variability. As an example, Figure 4 (right) depicts the probability density functions of the offset voltage of the operational amplifier after 1 year of operation as expected for different size transistors in the differential input stage. As an additional feature, the NBTI compact model takes into account varying operating conditions of the circuit like circuit off-times, different operating modes, dynamic voltage scaling, and temperature variations [8].

The implementation of this NBTI compact model is compatible with the reliability interfaces of the major design environments (Cadence URI, Synopsys MOSRA, Mentor Graphics UDRM, and the emerging TMI/OMI) to support every design team in performing accurate and consistent aging simulations. Taking into account NBTI variability does not introduce a significant overhead in comparison to the impact of process variability.

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SUMMARY

The reliability of integrated circuits has become a major criterion, especially in applications that are safety-critical or intended for long product lifetimes. To analyze the circuit reliability in the design phase already, circuit level aging simulations have to be performed. So far, their wide-spread use has been hindered by inconsistent and simplistic device degradation models. At Fraunhofer IIS/EAS, device degradation models at different levels of complexity and accuracy are set up, calibrated, and implemented with an equal support of multiple design environments to support designers in meeting their reliability targets.

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